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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/007,300
Filing Date ..... November 8, 2001
Inventor ..... Keiji Jono et al.
Assignee ..... KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit 2811
Examiner ..... T.F. Tran
Attorney's Docket No. KM1-003
Title: Trench-Isolated Transistors, Trench Isolation Structures, Memory Cells, and DRAMs (As Amended)

RESPONSE TO JANUARY 29, 2003 OFFICE ACTION

To: Mail Stop Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: D. Brent Kenady
Tel. 509-624-4276; Fax 509-838-3424
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601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Responsive to the Office Action dated January 29, 2003, Applicant amends and remarks as follows:

AMENDMENTS

Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

In th Title

~~Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS~~ Trench-Isolated Transistors, Trench Isolation Structures, Memory Cells, and DRAMs